Robert M. Radway

Ph.D. Candidate, Department of Electrical Engineering, Stanford University
radway@stanford.edu | +1-773-852-3830 | 353 Jane Stanford Way, Room 407, Stanford, CA 94305, USA

RESEARCH INTERESTS

Scaling VLSI systems via multiple multiplicative improvements: heterogeneous 2.5D, 3D, and monolithic 3D integration; technology-optimized VLSI chips for AI/ML, AR/VR, and the IoT; heterogenous-technology systems EDA & compilation.

EDUCATION

Stanford University, Ph.D. Candidate, EE (Advisor – Prof. Subhasish Mitra) 2018 – June 2024 (Expected)
Massachusetts Institute of Technology, B.S., M.Eng., EECS, (Advisor – Prof. Tomás Palacios) Feb 2016, Feb 2017

RESEARCH & WORK EXPERIENCE

Robust Systems Group, *Graduate Research Assistant* June 2018 – Present

Technology-Optimized VLSI Systems: Resistive RAM (RRAM) for edge AI/ML inference and training that scale.

- Developed multi-chip system for CHIMERA, a RRAM-based edge AI/ML SoC with peak 2.2 TOPS/W energy efficiency, edge incremental training, 33us wakeup/shutdown, scaled to 6× larger models with <4% exec. time and <5% energy overheads (**Symp. VLSI Circuits '21 – Joint Focus Session, Best Student Paper Award**, **JSSC '22, Equal Contrib.**).
- Physical design and custom 16-chip system integration of MINOTAUR, an RRAM-based, Transformer-optimized accelerator SoC for inference and training. Developed spatiotemporally fine-grained power gating for dynamically adjustable (< 1us), energy-proportional RRAM bandwidth (in preparation).

New Memories for Monolithic 3D: Optimized ultra-dense (monolithic) 3D ICs integrating RRAM & CNFETs on silicon.

- Iso-footprint and iso-capacity approach to 5-10× EDP benefits for monolithic 3D ICs (Carbon Nanotube FETs – CNFETs + RRAM + silicon CMOS) vs. 2D ICs (RRAM +silicon CMOS) (**DATE '23, Equal Contribution**).
- First iso-footprint, iso-node, iso-performance, iso-reliability CNFET-RRAM cell vs. Si-RRAM cell, with apples-to-apples (same wafer) measurement (**Symp. VLSI Technology & Circuits '23, Technology Focus Session, Equal Contrib.**).

3D MOSAIC (**M**onolithic, **S**tacked, **A**ssembled **IC**) Systems that Scale via Multiple Multiplicative Improvements:

- Developed Illusion Systems that create the illusion of large on-chip memory (i.e., energy and exec. time within 5% of a dream single chip). Developed heuristic and binary integer linear program partitioning for ML applications on Illusion Systems. Developed hardware platform and simulations to demonstrate Illusion (**Nature Electronics '21, First Author**).
- Developed Illusion Scaleup theory, finding linear improvement pathways in on-chip and inter-chip technology were sufficient to match exponential growth in ML application demands over a fixed horizon when combined with the Illusion Systems approach on a 3D MOSAIC (**IEDM '21, First Author**).
- Developed parameterized application-to-emulation flow to demonstrate Illusion Scaleup via cycle-accurate system emulation using HLS and a power-aware Illusion compiler (leveraging fine-grained spatiotemporal power gating on chip) to generate parameterized Illusion Systems with variable per-chip capacities and chip-to-chip links (in preparation).

Facebook/Meta Reality Labs, *Silicon Research Intern* *June 2021 – Jan 2022*

- Analyzed AR/VR applications via Illusion System approach for multi-chip scalability (**IEDM '21, First Author**).
- Analyzed design tradeoffs for 3D TSV-integrated SRAM memory in AR/VR systems (IEEE Micro '22).

D.E. Shaw & Co., *Asset Backed Securities Trader* *Jan 2017 – June 2018*

TEACHING, MENTORING, OUTREACH, PROFESSIONAL SERVICE

Stanford University, Guest Lecturer on Packaging, Design Projects in VLSI Systems I *Winter 2022, 2023*
Stanford University, Undergraduate/Master's Research Mentor *(>10 students including URM/FLI)* Sep 2018 – Present
Massachusetts Institute of Technology, Teaching Assistant, Intro to EECS I *(Median Rating 7/7)* *Fall 2013, Spring 2016*
Reviewer: DAC '23, ACM JETC, IEEE JSSC, IEEE TCAD, IEEE TCAS-II, IEEE TVLSI

PUBLICATIONS, PATENTS, PRESENTATIONS

Google Scholar: https://scholar.google.com/citations?user=Ec_V2HwAAAAJ&hl=en&oi=ao
Co-authored 16 peer-reviewed publications in journals (Nature Electronics, JSSC, EDL, IEEE TED, IEEE Micro) and conferences (Symp. VLSI Technology & Circuits, ISSCC, IEDM, DAC, DATE, ICCAD, ISQED) (over 200 citations, h-index of 8), along with a book chapter and patent application. Presented on work globally with over 20 presentations and posters.

HONORS & AWARDS

- **Cadence Design Systems Fellow (Stanford Graduate Fellowship)** Fall 2019 – Summer 2023
- **Stanford SystemX FMA Fellow** Fall 2019 – Present
- **MIT EECS – Mason Undergraduate Research and Innovation Scholar (SuperUROP)** Aug 2014 – May 2015